TX8M

Computer On Module

- Processor — 1.6GHz ARM® Cortex®-A53 based NXP i.MX 8M Mini
- RAM — 1GB DDR3L SDRAM
- ROM — 4GB eMMC
- Power supply — 3.3V to 5V
- Size — 26mm SO-DIMM
- Grade — Industrial
- Temperature — -25°C to 85°C



Key Features

- Quad Cortex-A53
- Display support:
  1x MIPI DSI (4-lane) display interface
  Vivante GC NanoUltra 3D + GC320 2D
  1080p video decode H.265, H.264, VP9, VP8
  1080p video encode H.264, VP8
- Camera Interfaces:
  1x MIPI CSI (4-lane) camera interface
- Cortex-M4 core for real-time processing

Connectivity

- 10/100Mbps Ethernet
- 2x USB
- 4x UART, 4x I²C, 3x SPI
- PCIe 2.0 (1-lane)
- 3.3V I/O

OS Support

- Linux

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Computer on module

The TX8M is a member of the TXCOM module series, specially designed for i.MX multimedia processors. TXCOM modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. With a focus on longevity TXCOM modules includes an i.MX processor, power supply and memory.

The i.MX 8M Mini is NXP's first embedded multi-core heterogeneous applications processors built using advanced 14LPC FinFET process technology. The i.MX 8M Mini family of processors brings together high-performance computing, power efficiency, enhanced system reliability and embedded security needed to drive the growth of fast-growing edge node computing, streaming multimedia, and machine learning applications.

At the heart is a scalable core complex of up to four Arm® Cortex®-A53 cores plus Cortex®-M4 based real-time processing domain at 400+MHz. i.MX 8M Mini core options are optimized for low-power but offer the breadth of processing power necessary for consumer, audio, industrial, machine learning training and inferencing across a range of cloud providers. The i.MX 8M Mini also packs-in hardware 1080p video acceleration to enable two-way video applications, 2D and 3D graphics to provide a rich visual HMI experience, and advanced audio capabilities to enable audio-rich applications. An extensive selection of high-speed interfaces enabling broader system connectivity, and targeting industrial level qualification, the i.MX 8M Mini family may be used in any general embedded consumer and industrial application.

- NXP i.MX 8M Mini Quad, 1GB DDR3L SDRAM
- 4GB eMMC
- DIMM200-module (67,6mm x 26 mm x 4mm)
- Operation temperature up to 105°C (processor junction temp.)

Standard TXCOM pinout:

Highly scalable design options allow a single platform to cover multiple products. Pin-compatible TX modules allow a single PCB as a platform for different features as product needs dictate.

- 4-wire UARTs (x3)
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

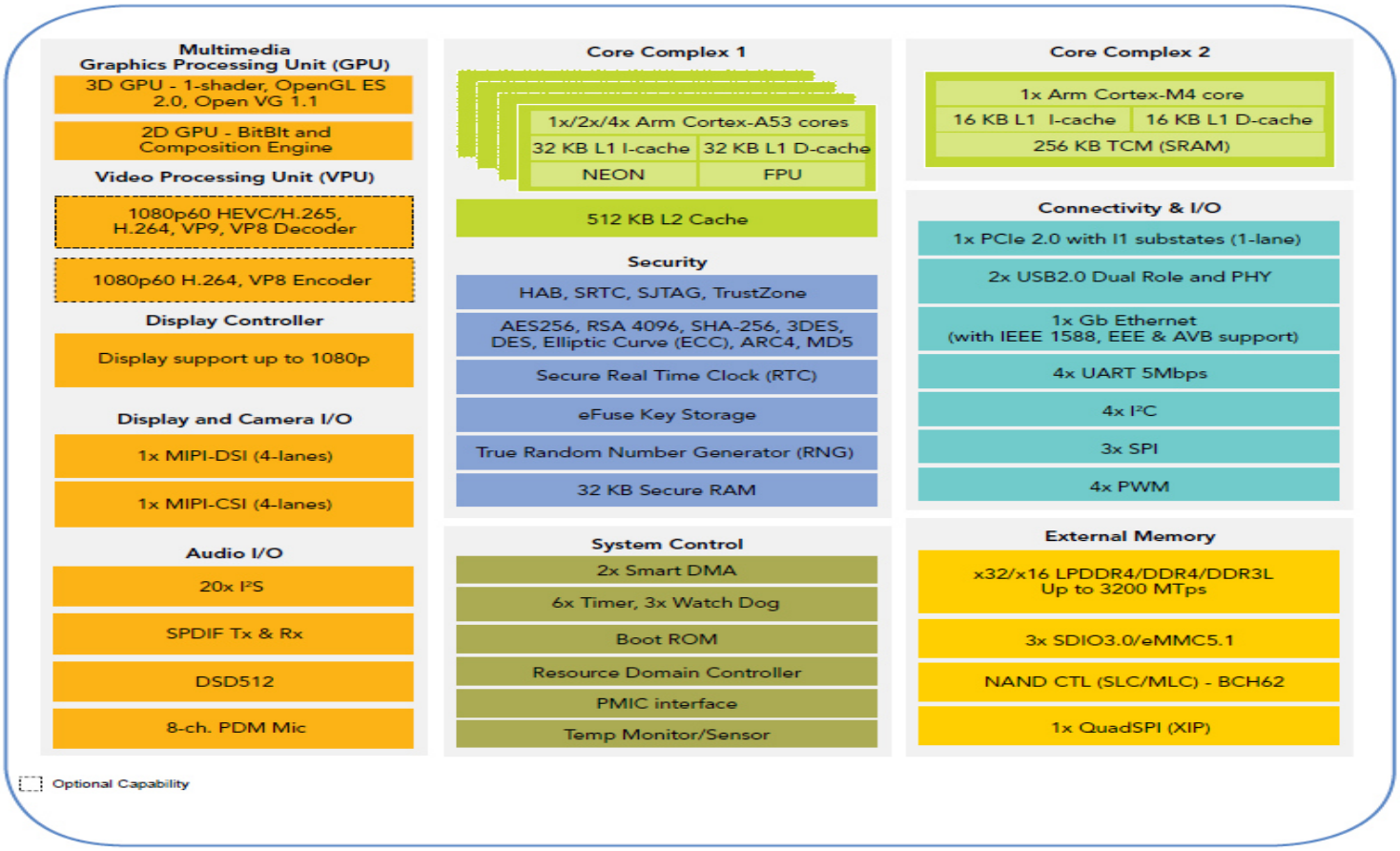
High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide

i.MX 8M MINI FAMILY BLOCK DIAGRAM



Order Number	CPU	SDRAM	Flash
TX8MMQ/1024S/4GF/E85	1.6 GHz i.MX 8M Mini Quad	1GB	4GB

2019-01-07

PINOUT

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input.
5-7, 9-12	power	VOUT				3.3V power supply output. Supplied by SW7
8	3V3	BOOTMODE				Boot mode select H: Boot from eMMC / L: Boot from UART/USB
13	Not connected					
14	Not connected					
15	3V3	#RESET_OUT	SD2_RESET_B	USDHC2_RESET_B, SRC_SYSTEM_RESET	GPIO2[19]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime.
16		#POR	Connected to PMIC: PWRON_B		10K-PU to VIN	Power On Reset — Active low input signal Leave unconnected, if not used.
17	3V3	#RESET_IN	Connected to PMIC: WDOG_B		10K-PU to 3V3	WDOG_B is an active-low input for triggering Cold Reset or Warm Reset. Refer to BD71847MWV Datasheet.
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	GPIO1_IO14	USB2_OTG_PWR, USDHC3_CD_B, PWM3_OUT, CCM_CLKO1	GPIO1[14] 10K-PU	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	GPIO1_IO15	USB2_OTG_OC, USDHC3_WP, PWM4_OUT, CCM_CLKO2	GPIO1[15] 10K-PU	Active low over-current indicator input connected to a GPIO.
29	analog	USBH_DM	USB2_DN			D- pin of the USB cable
30	analog	USBH_VBUS	USB2_VBUS			USB supply voltage
31	analog	USBH_DP	USB2_DP			D+ pin of the USB cable
32	GND	GND				
USB-OTG						
33	3V3	USBOTG_ID	USB1_ID			
34	3V3	USBOTG_VBUSEN	GPIO1_IO12	USB1_OTG_PWR, SDMA2_EXT_EVENT1	GPIO1[12] 10K-PU	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	USB1_DN			D- pin of the USB cable
36	3V3	#USBOTG_OC	GPIO1_IO13	USB1_OTG_OC, PWM2_OUT	GPIO1[13] 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	USB1_DP			D+ pin of the USB cable
38	analog	USBOTG_VBUS	USB1_VBUS			USB supply voltage
39	GND	GND				
I2C						
40	3V3	I2C_DATA	I2C2_SDA	ENET1_1588_EVENT1_OUT, USDHC3_WP	GPIO5[17]	I2C Data
41	3V3	I2C_CLK	I2C2_SCL	ENET1_1588_EVENT1_IN USDHC3_CD_B	GPIO5[16]	I2C Clock
PWM						
42	3V3	PWM	GPIO1_IO01	PWM1_OUT, XTALOSC_REF_CLK_24M, CCM_EXT_CLK2	GPIO1[01]	PWM Output

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
1-WIRE						
43	3V3	OWDAT	SAI5_MCLK	SAI5_MCLK, SAI1_TX_BCLK	GPIO3[25]	
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	ECSPI2_SS0	ECSPI2_SS0, UART4_RTS_B	GPIO5[13]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS	SD2_WP	USDHC2_WP	GPIO2[20]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	ECSPI2_MOSI	ECSPI2_MOSI, UART4_TX	GPIO5[11]	Master Out/Slave In signal
47	3V3	CSPI_MISO	ECSPI2_MISO	ECSPI2_MISO, UART4_CTS_B	GPIO5[12]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	ECSPI2_SCLK	ECSPI2_SCLK, UART4_RX	GPIO5[10]	Serial Clock signal
49	Not connected					
50	GND	GND				
1st SD – Secure Digital Interface						
51	3V3	SD1_CD	SD2_CD_B	USDHC2_CD_B	GPIO2[12]	SD Card Detect
52	3V3	SD1_D[0]	SD2_DATA0	USDHC2_DATA0	GPIO2[15]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D[1]	SD2_DATA1	USDHC2_DATA1	GPIO2[16]	
54	3V3	SD1_D[2]	SD2_DATA2	USDHC2_DATA2	GPIO2[17]	
55	3V3	SD1_D[3]	SD2_DATA3	USDHC2_DATA3	GPIO2[18]	
56	3V3	SD1_CMD	SD2_CMD	USDHC2_CMD	GPIO2[14]	SD Command bidirectional signal
57	3V3	SD1_CLK	SD2_CLK	USDHC2_CLK	GPIO2[13]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	TXD	UART1_TXD	UART1_TX, ECSPI3_MOSI	GPIO5[23]	Application UART 1 Transmit Data output signal
60	3V3	RXD	UART1_RXD	UART1_RX, ECSPI3_SCLK	GPIO5[22]	Application UART 1 Receive Data input signal
61	3V3	RTS	UART3_TXD	UART3_TX, UART1_RTS_B, USDHC3_VSELECT	GPIO5[27]	Application UART 1 Request to Send **input** signal
62	3V3	CTS	UART3_RXD	UART3_RX, UART1_CTS_B, USDHC3_RESET_B	GPIO5[26]	Application UART 1 Clear to Send **output** signal
2nd UART						
63	3V3	TXD	UART2_TXD	UART2_TX, ECSPI3_SS0	GPIO5[25]	Application UART 2 Transmit Data output signal
64	3V3	RXD	UART2_RXD	UART2_RX, ECSPI3_MISO	GPIO5[24]	Application UART 2 Receive Data input signal
65	3V3	RTS	UART4_TXD	UART4_TX, UART2_RTS_B	GPIO5[29]	Application UART 2 Request to Send **input** signal
66	3V3	CTS	UART4_RXD	UART4_RX, UART2_CTS_B, PCIE1_CLKREQ_B	GPIO5[28]	Application UART 2 Clear to Send **output** signal
3rd UART						
67	3V3	TXD	ECSPI1_MOSI	ECSPI1_MOSI, UART3_TX	GPIO5[07]	Application UART 3 Transmit Data output signal
68	3V3	RXD	ECSPI1_SCLK	ECSPI1_SCLK, UART3_RX	GPIO5[06]	Application UART 3 Receive Data input signal
69	3V3	RTS	ECSPI1_SS0	ECSPI1_SS0, UART3_RTS_B	GPIO5[09]	Application UART 3 Request to Send **input** signal
70	3V3	CTS	ECSPI1_MISO	ECSPI1_MISO, UART3_CTS_B	GPIO5[08]	Application UART 3 Clear to Send **output** signal
71	GND	GND				

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
Module Specific Signals						
72	3V3		SAI5_RXC	SAI5_RX_BCLK, SAI1_TX_DATA1, PDM_CLK	GPIO3[20]	
73	3V3		SAI5_RXD0	SAI5_RX_DATA0, SAI1_TX_DATA2, PDM_BIT_STREAM0	GPIO3[21]	
74	3V3		SAI5_RXD1	SAI5_RX_DATA1, SAI1_TX_DATA3, SAI1_TX_SYNC, SAI5_TX_SYNC, PDM_BIT_STREAM1	GPIO3[22]	
75	3V3		SAI5_RXD2	SAI5_RX_DATA2, SAI1_TX_DATA4, SAI1_TX_SYNC, SAI5_TX_BCLK, PDM_BIT_STREAM2	GPIO3[23]	
76	3V3		SAI5_RXD3	SAI5_RX_DATA3, SAI1_TX_DATA5, SAI1_TX_SYNC, SAI5_TX_DATA0, PDM_BIT_STREAM3	GPIO3[24]	
77	3V3		SAI5_RXFS	SAI5_RX_SYNC, SAI1_TX_DATA0	GPIO3[19]	
78	3V3		SAI2_RXC	SAI2_RX_BCLK, SAI5_TX_BCLK, UART1_RX	GPIO4[22]	
79	3V3		SAI2_RXFS	SAI2_RX_SYNC, SAI5_TX_SYNC, SAI5_TX_DATA1, SAI2_RX_DATA1, UART1_TX	GPIO4[21]	
80	3V3		SAI3_RXC	SAI3_RX_BCLK, GPT1_CLK, SAI5_RX_BCLK, UART2_CTS_B	GPIO4[29]	
81	3V3		SAI3_RXFS	SAI3_RX_SYNC, GPT1_CAPTURE1, SAI5_RX_SYNC, SAI3_RX_DATA1	GPIO4[28]	
82	GND	GND				
1st SSI - Serial Audio Port						
83	3V3	SSI1_INT	SAI2_MCLK	SAI2_MCLK, SAI5_MCLK	GPIO4[27]	
84	3V3	SSI1_RXD	SAI2_RXD0	SAI2_RX_DATA0, SAI5_TX_DATA0, UART1_RTS_B	GPIO4[23]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	SAI2_TXD0	SAI2_TX_DATA0, SAI5_TX_DATA3	GPIO4[26]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	SAI2_TXC	SAI2_TX_BCLK, SAI5_TX_DATA2	GPIO4[25]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	SAI2_TXFS	SAI2_TX_SYNC, SAI5_TX_DATA1, SAI2_TX_DATA1, UART1_CTS_B	GPIO4[24]	Serial Audio Interface left/right clock
88	GND	GND				
2nd SSI - Serial Audio Port						
89	3V3	SSI2_INT	SAI3_MCLK	SAI3_MCLK, PWM4_OUT, SAI5_MCLK	GPIO5[02]	
90	3V3	SSI2_RXD	SAI3_RXD	SAI3_RX_DATA0, GPT1_COMPARE1, SAI5_RX_DATA0, UART2_RTS_B	GPIO4[30]	Serial Audio Interface serial data line 1
91	3V3	SSI2_TXD	SAI3_TXD	SAI3_TX_DATA0, GPT1_COMPARE3, SAI5_RX_DATA3	GPIO5[01]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	SAI3_TXC	SAI3_TX_BCLK, GPT1_COMPARE2, SAI5_RX_DATA2, UART2_TX	GPIO5[00]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	SAI3_TXFS	SAI3_TX_SYNC, GPT1_CAPTURE2, SAI5_RX_DATA1, SAI3_TX_DATA1, UART2_RX	GPIO4[31]	Serial Audio Interface left/right clock
94	GND	GND				

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
2nd SD – Secure Digital Interface						
95	3V3	SD2_CD	NAND_DATA02	RAWNAND_DATA02, QSPI_A_DATA2, USDHC3_CD_B	GPIO3[08]	
96	3V3	SD2_D[0]	NAND_DATA04	RAWNAND_DATA04, QSPI_B_DATA0, USDHC3_DATA0	GPIO3[10]	
97	3V3	SD2_D[1]	NAND_DATA05	RAWNAND_DATA05, QSPI_B_DATA1, USDHC3_DATA1	GPIO3[11]	
98	3V3	SD2_D[2]	NAND_DATA06	RAWNAND_DATA06, QSPI_B_DATA2, USDHC3_DATA2	GPIO3[12]	
99	3V3	SD2_D[3]	NAND_DATA07	RAWNAND_DATA07, QSPI_B_DATA3, USDHC3_DATA3	GPIO3[13]	
100	3V3	SD2_CMD	NAND_WP_B	RAWNAND_WP_B, USDHC3_CMD	GPIO3[18]	
101	3V3	SD2_CLK	NAND_WE_B	RAWNAND_WE_B, USDHC3_CLK	GPIO3[17]	
102	GND	GND				
Module Specific Signals						
103	3V3		NAND_ALE	RAWNAND_ALE, QSPI_A_SCLK	GPIO3[00]	
104	3V3		NAND_CE0_B	RAWNAND_CE0_B, QSPI_A_SS0_B	GPIO3[01]	
105	3V3		NAND_CE1_B	RAWNAND_CE1_B, QSPI_A_SS1_B, USDHC3_STROBE	GPIO3[02]	
106	3V3		NAND_CE2_B	RAWNAND_CE2_B, QSPI_B_SS0_B, USDHC3_DATA5	GPIO3[03]	
107	3V3		NAND_CE3_B	RAWNAND_CE3_B, QSPI_B_SS1_B, USDHC3_DATA6	GPIO3[04]	
108	3V3		NAND_DATA00	RAWNAND_DATA00, QSPI_A_DATA0	GPIO3[06]	
109	3V3		NAND_DATA01	RAWNAND_DATA01, QSPI_A_DATA1	GPIO3[07]	
110	3V3		NAND_DATA03	RAWNAND_DATA03, QSPI_A_DATA3, USDHC3_WP	GPIO3[09]	
111	GND	GND				
112	3V3		NAND_CLE	RAWNAND_CLE, QSPI_B_SCLK, USDHC3_DATA7	GPIO3[05]	
113	3V3		NAND_DQS	RAWNAND_DQS, QSPI_A_DQS	GPIO3[14]	
114	3V3		NAND_RE_B	RAWNAND_RE_B, QSPI_B_DQS, USDHC3_DATA4	GPIO3[15]	
115	3V3		NAND_READY_B	RAWNAND_READY_B, USDHC3_RESET_B	GPIO3[16]	
116	GND	GND				

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
MIPI						
117	LVDS		MIPI_DSI_D2_N			
118	LVDS		MIPI_DSI_D1_N			
119	LVDS		MIPI_DSI_D2_P			
120	LVDS		MIPI_DSI_D1_P			
121	LVDS		MIPI_DSI_D3_N			
122	LVDS		MIPI_DSI_D0_N			
123	LVDS		MIPI_DSI_D3_P			
124	LVDS		MIPI_DSI_D0_P			
125	LVDS		MIPI_DSI_CLK_N			
126	LVDS		MIPI_CSI_D3_P			
127	LVDS		MIPI_DSI_CLK_P			
128	LVDS		MIPI_CSI_D3_N			
129	GND	GND				
130	LVDS		MIPI_CSI_CLK_P			
131	LVDS		MIPI_CSI_D2_P			
132	LVDS		MIPI_CSI_CLK_N			
133	LVDS		MIPI_CSI_D2_N			
134	LVDS		MIPI_CSI_D1_P			
135	LVDS		MIPI_CSI_D0_P			
136	LVDS		MIPI_CSI_D1_N			
137	LVDS		MIPI_CSI_D0_N			
138	Not connected					
139	Not connected					
140	Not connected					
141	Not connected					
142	GND	GND				
143	3V3		SPDIF_RX	SPDIF1_IN, PWM2_OUT	GPIO5[04]	
144	3V3		SPDIF_TX	SPDIF1_OUT, PWM3_OUT	GPIO5[03]	
145	Not connected					
146	3V3		SPDIF_EXT_CLK	SPDIF1_EXT_CLK, PWM1_OUT	GPIO5[05]	
147	GND	GND				
Module Specific Signals						
148	3V3		I2C3_SCL	I2C3_SCL, PWM4_OUT, GPT2_CLK	GPIO5[18]	
149	3V3		I2C3_SDA	I2C3_SDA, PWM3_OUT, GPT3_CLK	GPIO5[19]	
150	3V3		I2C4_SCL	I2C4_SCL, PWM2_OUT, PCIE1_CLKREQ_B	GPIO5[20]	
151	3V3		I2C4_SDA	I2C4_SDA, PWM1_OUT	GPIO5[21]	
152	3V3		GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT, XTALOSC_REF_CLK_32K, CCM_EXT_CLK1	GPIO1[00]	

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
153	3V3		GPIO1_IO02	WDOG1_WDOG_B, WDOG1_WDOG_ANY, SJC_DE_B	GPIO1[02]	
154	3V3		GPIO1_IO04	USDHC2_VSELECT, SDMA1_EXT_EVENT1	GPIO1[04]	
155	3V3		GPIO1_IO05	M4_NMI, CCM_PMIC_READY	GPIO1[05]	
156	3V3		GPIO1_IO06	ENET1_MDC, USDHC1_CD_B, CCM_EXT_CLK3	GPIO1[06]	
157	3V3		GPIO1_IO07	ENET1_MDIO, USDHC1_WP, CCM_EXT_CLK4	GPIO1[07]	
158	3V3		GPIO1_IO08	ENET1_1588_EVENT0_IN USDHC2_RESET_B	GPIO1[08]	
159	3V3		GPIO1_IO09	ENET1_1588_EVENT0_OUT, USDHC3_RESET_B, SDMA2_EXT_EVENT0	GPIO1[09]	
160	GND	GND				
161	3V3		GPIO1_IO10	USB1_OTG_ID	GPIO1[10]	
162	3V3		GPIO1_IO11	USB2_OTG_ID, USDHC3_VSELECT, CCM_PMIC_READY	GPIO1[11]	
163	Not connected					
164	Not connected					
165	Not connected					
166	LVDS		PCIE_CLK_P			
167	LVDS		PCIE_RXN_N			
168	LVDS		PCIE_CLK_N			
169	LVDS		PCIE_RXN_P			
170	LVDS		PCIE_TXN_N			
171	GND	GND				
172	LVDS		PCIE_TXN_P			
173	Not connected					
174	Not connected					
175	Not connected					
176	Not connected					
177	Not connected					
178	3V3		SAI1_RXFS	SAI1_RX_SYNC, SAI5_RX_SYNC, CORESIGHT_TRACE_CLK	GPIO4[00]	
179	3V3		SAI1_TXFS	SAI1_TX_SYNC, SAI5_TX_SYNC, CORESIGHT_EVENTO	GPIO4[10]	
180	3V3		SAI1_RXC	SAI1_RX_BCLK, SAI5_RX_BCLK, CORESIGHT_TRACE_CTL	GPIO4[01]	
181	3V3		SAI1_TXC	SAI1_TX_BCLK, SAI5_TX_BCLK, CORESIGHT_EVENTI	GPIO4[11]	
182	3V3		SAI1_MCLK	SAI1_MCLK, SAI5_MCLK, SAI1_TX_BCLK, PDM_CLK	GPIO4[20]	
183	GND	GND				
184	3V3		SAI1_RXD0	SAI1_RX_DATA0, SAI5_RX_DATA0, SAI1_TX_DATA1, PDM_BIT_STREAM0, CORESIGHT_TRACE0	GPIO4[02]	
185	3V3		SAI1_RXD1	SAI1_RX_DATA1, SAI5_RX_DATA1, PDM_BIT_STREAM1, CORESIGHT_TRACE1	GPIO4[03]	

PIN	Type	TX Standard	i.MX8MM Pad Name	Alternate functions	GPIO	Description (refer to i.MX8MM manuals for details)
186	3V3		SAI1_RXD2	SAI1_RX_DATA2, SAI5_RX_DATA2, PDM_BIT_STREAM2, CORESIGHT_TRACE2	GPIO4[04]	
187	3V3		SAI1_RXD3	SAI1_RX_DATA3, SAI5_RX_DATA3, PDM_BIT_STREAM3, CORESIGHT_TRACE3	GPIO4[05]	
188	3V3		SAI1_RXD4	SAI1_RX_DATA4, SAI6_TX_BCLK, SAI6_RX_BCLK, CORESIGHT_TRACE4	GPIO4[06]	
189	3V3		SAI1_RXD5	SAI1_RX_DATA5, SAI6_TX_DATA0, SAI6_RX_DATA0, SAI1_RX_SYNC, CORESIGHT_TRACE5	GPIO4[07]	
190	3V3		SAI1_RXD6	SAI1_RX_DATA6, SAI6_TX_SYNC, SAI6_RX_SYNC, CORESIGHT_TRACE6	GPIO4[08]	
191	3V3		SAI1_RXD7	SAI1_RX_DATA7, SAI6_MCLK, SAI1_TX_SYNC, SAI1_TX_DATA4, CORESIGHT_TRACE7	GPIO4[09]	
192	3V3		SAI1_TXD0	SAI1_TX_DATA0, SAI5_TX_DATA0, CORESIGHT_TRACE8	GPIO4[12]	
193	3V3		SAI1_TXD1	SAI1_TX_DATA1, SAI5_TX_DATA1, CORESIGHT_TRACE9	GPIO4[13]	
194	3V3		SAI1_TXD2	SAI1_TX_DATA2, SAI5_TX_DATA2, CORESIGHT_TRACE10	GPIO4[14]	
195	3V3		SAI1_TXD3	SAI1_TX_DATA3, SAI5_TX_DATA3, CORESIGHT_TRACE11	GPIO4[15]	
196	3V3		SAI1_TXD4	SAI1_TX_DATA4, SAI6_RX_BCLK, SAI6_TX_BCLK, CORESIGHT_TRACE12	GPIO4[16]	
197	3V3		SAI1_TXD5	SAI1_TX_DATA5, SAI6_RX_DATA0, SAI6_TX_DATA0, CORESIGHT_TRACE13	GPIO4[17]	
198	3V3		SAI1_TXD6	SAI1_TX_DATA6, SAI6_RX_SYNC, SAI6_TX_SYNC, CORESIGHT_TRACE14	GPIO4[18]	
199	3V3		SAI1_TXD7	SAI1_TX_DATA7, SAI6_MCLK, PDM_CLK, CORESIGHT_TRACE15	GPIO4[19]	
200	GND	GND				